A Single Chip FSK/ASK 900MHz Transceiver in a Standard 0.25um CMOS Technology

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Abstract — **This paper presents a low power consumption single chip FSK/ASK transceiver for half-duplex low datarate communication in the 868-870MHz band. The IC was processed in a standard 0.25um CMOS technology, offers a very high level of integration and needs only few external components. The transmit/receive RF front end contains a high efficiency power amplifier, a low noise amplifier (LNA), a double balanced RF mixer and an I/Q mixer for down conversion to an intermediate frequency (IF) of 289MHz and further to zero IF. The transmit/receive frequency synthesis of 868/1157MHz is done by a fully integrated switchable frequency range voltage controlled oscillator (VCO), a phase locked loop synthesizer (PLL) and a tunable crystal oscillator used as reference frequency generator as well as FSK modulator. A bandwidth configurable I/Q channel select filter, an I/Q limiter with RSSI generation used also for AM demodulation, a FSK demodulator, a bandwidth configurable data filter and a dataslicer is implemented for further zero IF and baseband analog signal processing. The transceiver can be configured by a 2/3-wire bus interface. Low-drop voltage regulators are implemented to allow supply voltages up to 3.6V because the maximum allowed voltages for the standard MOS transistors are 2.8V. The overall current consumption of the transceiver in the receive and transmit mode is 11mA and 20mA, respectively. Additionally, a standby mode and idle mode is realized to increase battery lifetime.**

I. INTRODUCTION

A solution is presented which is adopted for high volume consumer products in the 868MHz European ISM (Industrial, Scientific, and Medical) band. Many applications like home automation, alarm systems or industrial control share the need for small sized, low cost and low power transceivers. Current consumption of less than 10mA in the receive mode respectively 20mA in the transmit mode are typical by achieving a receiver sensitivity of at least –100dBm with data rates up to 30kbit/s. Transmitter output power up to 10dBm is required. A power supply voltage range from 2.1V up to 3.6V is not uncommon for these battery powered applications.

The cost and volume requirements favor a solution with a high degree of integration in a standard CMOS process. Recent works have shown that a low power consumption is feasible by using submicron CMOS processes.

The architecture and building blocks of the transceiver are described in the following sections. Finally, measurement results of the fabricated transceiver are presented.

II. CHIP ARCHITECTURE

A block diagram of the transceiver is shown in Figure 1. The main parts are the receiver, the frequency synthesizer, the power amplifier and circuits like voltage regulators, a bandgap reference and a serial bus interface.

The ASK/FSK receiver uses a dual conversion to zero IF architecture [1] [2]. One reason for this concept is that flicker noise appears at the output of a down conversion mixer [3]. To reduce this flicker noise the LO amplitude and the size of the mixer switches have to be raised resulting in an increased LO buffer load and thus power consumption. To circumvent the problem a dual conversion receiver was implemented. The RF frequency is first down converted to an IF frequency and furthermore to zero IF. The relationship between LO frequency f_{LO}, the RF frequency f_{RF} and the IF frequency f_{IF} is given by

$$f_{LO} = 4/3\, f_{RF} = 4\, f_{IF} \qquad (1)$$

With this choice a compromise between power consumption, image rejection and flicker noise suppression was achieved. Only one VCO is needed as additional benefit since the IF frequency can be easily generated by a divider. The image frequency is located well away, which results in less RF filtering effort. Also the LO leakage is reduced since the RF filter blocks a significant portion of the LO interference. Differential RF input and dual conversion architecture remedies undesired AM demodulation by second order distortion.

The zero IF circuits comprise a channel select filter, a limiter and a frequency shift keying FSK demodulation for the I/Q channels. The bandwidth of the channel select filter is configurable to accomplish different adjacent channel rejections, frequency modulation indexes and

datarates. DC offset can be removed by a capacitvely coupled limiter since FSK modulation is used. An on chip quadrature correlator is used for FSK demodulation. The RSSI block of the limiter is used for AM demodulation.

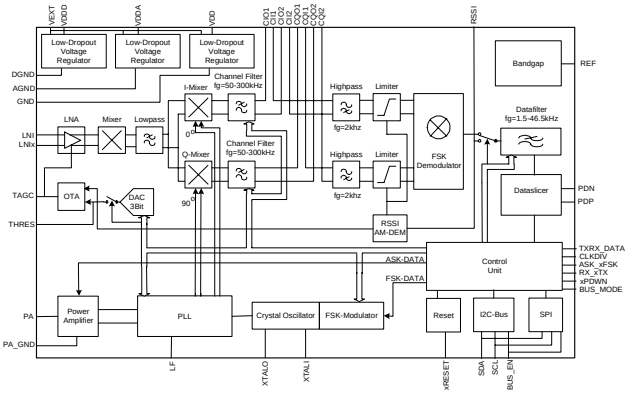

Fig. 1. 900MHz FSK/ASK Transceiver block diagram.

Further baseband processing is done by a datafilter with configurable bandwidth to achieve optimum performance for datarates between 1kbit/s up to 30 kbit/s. A dataslicer is used for digital signal recovering.

A frequency synthesizer is realized to generate the transmit/receive frequencies. The frequency range of the VCO and the divider ratio can be switched to achieve this.

A power amplifier is implemented for the ASK/FSK transmitter. The ASK modulation is done by on/off switching of the power amplifier. The FSK modulation is accomplished by pulling the crystal oscillator.

A supply voltage range from 2.1V to 3.6V was specified for the transceiver. For that reason low-drop voltage regulators were implemented to allow a supply voltage higher than the allowed voltages for the standard MOS transistors of 2.8V. A standby mode is realized with a low power voltage regulator. This regulator is necessary in order that the configuration registers do not lose their content. The regulator draws a current of less than 100nA. An idle mode is also available where the crystal oscillator and the bus interface stay active.

The transceiver is configurable via a SPI or I2C-Bus. A default configuration is realized for applications without bus interface.

II. BUILDING BLOCKS

A. High Frequency Front End

The differential low noise amplifier (LNA) is a common gate type. A constant gm cell to minimize gain and input impedance variations biases the LNA. A differential input impedance of 180Ω was chosen to reduce the power consumption of the LNA. The voltage gain is 20dB. A noise figure of 4.2dB and an IIP3 of –2dB were simulated. The LNA gain can be continuously attenuated to 0dB by a control loop to extend the dynamic range of the receiver. The threshold voltage can be set by a DAC and this voltage is compared with the received signal strength indicator level (RSSI) from the limiter. In case that the RSSI level is higher than the threshold voltage, the LNA gain is reduced and vice versa. The time constant of the AGC action can be determined by an external capacitor and should be chosen along with the appropriate threshold voltage according to the intended operating case and interference scenario to be expected during operation.

The double balanced RF mixer down converts the input frequency (RF) in the band of 868-870MHz to the intermediate frequency (IF) of approximately 289MHz. The local oscillator frequency (LO) is 1157MHz. A conversion voltage gain of 11dB, a noise figure of 16dB and an IIP3 of 5dB were simulated. The mixer is followed by a low pass filter with a corner frequency of approximately 350MHz in order to prevent RF and LO signals to appear at the intermediate frequency (IF).

The I/Q mixer comprises two identical double balanced mixers driven by the divide-by-four local oscillator signal. Each mixer has a conversion voltage gain of 9dB, a noise figure of 25dB and an IIP3 of 15dB. A square-wave LO with sharp transitions and appropriate area of the switches were chosen to minimize the flicker noise output.

B. Zero IF Implementation

The required adjacent channel rejection specifies the filter order for the channel select filter. Two 7th order low pass filters with butterworth characteristic were designed for the I/Q channel. Continuous time RC filters were used because of the high dynamic range requirements. The resistor value was chosen to meet the noise and power constraints. Mainly MOS capacitors with their inherent high area capacitance were used to reduce the required chip area. The filter linearity is still high enough not to limit the receiver linearity. The complex poles are accomplished by three Sallen-Key biquads. A passive pole is realized in the I/Q mixer. The bandwidth of the filters can be adjusted between 50kHz and 300kHz in 50kHz steps by switching the resistor values of the filter.

The I/Q limiters are AC coupled multistage amplifiers with a cumulative gain of approximately 85dB and a bandwidth of 1 MHz. Receive Signal Strength Indicator (RSSI) generators are included for the I/Q channel. The RSSI signals are summed up to build the nominal RSSI signal. This signal is used to demodulate ASK signals and to control the LNA gain.

C. Baseband Circuits

A quadrature correlator is used to demodulate frequency shift keyed (FSK) signals [4]. The sensitivity of the demodulator is 1mV/kHz over the maximum channel filter bandwidth of 300kHz.

A 2nd order Sallen-Key type data filter was used. The bandwidth can be adjusted between 1.5KHz and 46.5kHz in 1.5kHz steps.

The dataslicer is a fast comparator. A low pass mode and a peak detector mode for fast-attack and slow-release of the data signal is implemented to generate the self-adjusting threshold voltage. The time constant can be changed by an external capacitor.

D. Frequency Synthesizer

A Pierce type quartz oscillator was chosen as reference frequency. Fine tuning and FSK modulation can be achieved by pulling its frequency from the nominal operating frequency of about 18MHz by an internal capacitor bank. Frequency deviations of up to 100KHz can be achieved for the RF frequency.

The integer Phase Locked Loop (PLL) synthesizer consists of a fully integrated, switchable frequency range voltage controlled oscillator (VCO), a divider by four, an asynchronous divider chain (divide by 12 or 16), a phase detector with charge pump and an external loop filter.

The VCO is built around an on-chip octagonal balanced inductor [5]. The center frequency of the VCO in the transmit/receive mode is 868MHz/1156MHz. Switching capacitors parallel to the resonance tank change it. A depletion-mode PMOS tuning element was used to fine-tune the VCO. The size of tuning range was chosen to cover process tolerances. An amplitude regulation is implemented to achieve optimal power consumption for a given amplitude value which was chosen large enough to switch the mixer and frequency divider. The VCO receive and transmit phase noise fully meets consumer market demands.

The divider by four was built with two master-slave flip-flops, each realized with a current-steering differential latch. The outputs are inherently 90° out of phase, which are used to drive the I/Q mixers. The overall division ratio is 48 in the transmit mode and 64 in the receive mode.

E. Power Amplifier

The power amplifier is implemented as a two stage, class C amplifier. The first stage is a limiting differential amplifier with a class AB output buffer. The class C output amplifier is a large open-drain device. The load-and matching network is external. ASK modulation is realized by on/off switching of the power amplifier. Special care in the power supply, layout and design was taken to isolate the VCO from the power amplifier in order to reduce frequency pulling. Additionally, an isolation buffer was inserted between the VCO and the power amplifier.

F. Other Building Blocks

Additional circuits like the supply voltage regulators, the bandgap reference for biasing, power on reset and the bus interface were implemented.

One of the major concerns in a production line is the ESD robustness. New ESD concepts were devised to protect the RF circuits like the LNA and power amplifier. ESD protection up to 2KV HBM could be achieved.

III. Measurement results

The transceiver was fabricated in the Infineon C9N 0.25um CMOS process. A chip photograph of the complete chip is shown in Fig.2.

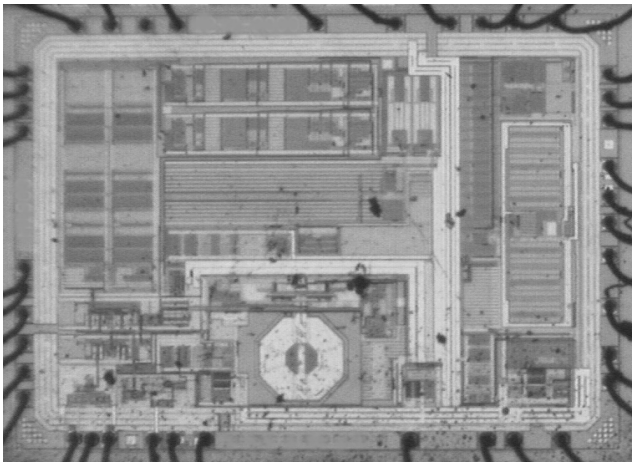

Fig. 2. 900MHz FSK/ASK Transceiver chip photograph

A. Receiver Measurements

The overall current drain of the transceiver in the receiver mode is 11mA. The measured performance is summarized in Table I.

TABLE I
MEASURED PERFORMANCE OF THE RECEIVER

	Measurements results		Unit
	High gain	Low gain	
Noise figure	11.8	N/A	dB
Input return loss	-17		dB
Differential gain	36	16	dB
I1dBCP	-31	-11	dBm
IIP3	-23.2	-3.5	dBm

Sensitivity measurements for ASK/FSK modulated signals with different Manchester coded datarates are shown in Table II and Table III.

TABLE II
ASK SENSITIVITY OF THE RECEIVER

Datarate	Datafilter bandwidth	Channel select filter bandwidth	ASK-Sensitivity BER<10^{-2}
[kbit/s]	[kHz]	[kHz]	[dBm]
2	4,5	520	-106
		270	-107
		110	-106
10	31,5	520	-94
		270	-95
		110	-97

TABLE III
FSK SENSITIVITY OF THE RECEIVER

Datarate	Datafilter bandwidth	Channel select filter bandwidth	FSK frequency deviation	FSK sensitivity BER<10^{-2}
[kbit/s]	[kHz]	[kHz]	[kHz]	[dBm]
2	4,5	520	10	-96
			30	-100
			100	-103
		270	10	-97
			30	-100
			100	-104
		110	30	-101
			50	-102
10	31,5	520	50	-96
			100	-97
			150	-97
		270	100	-99
30	46,5	520	150	-95
		270	150	-95

B. Transmitter Measurements

The overall current drain of the transceiver in the transmit mode is 20mA. An output power up to 10dBm into 50Ω was measured with a power-added efficiency of 32% at 3V-supply voltage. The radiation spectrum and spurious emissions are well below the out of band radiation limits.

C. Frequency Synthesizer

Frequency pulling greater than 120ppm was achieved on the 18MHz quartz reference oscillator.

A loop filter was chosen for a PLL closed loop bandwidth of 150kHz. An inloop PLL phase noise of -85dBc/Hz was measured. The reference spurious of the PLL is less than -65dBc.

The VCO tuning range in both frequency ranges is 17%. A open loop VCO phase noise of –95dBc@100kHz was achieved.

VI. CONCLUSION

It was shown that submicron CMOS processes are well suited for consumer products in the 868MHz European ISM band. A high sensitivity with a reasonable power consumption was achieved. For that reason, CMOS RF products for the consumer market are expected in the future.

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REFERENCES

[1] A.A.Abidi and H.Darabi, "Low Power RF Integrated Circuits: Principles and Practice," in the *Int'l Symp. On Low Power Electronics & Design proceedings*, pp. 1-6, Aug. 1999.

[2] Sergio A. Sanielevici et.al.,"A 900 MHz Transceiver Chipset for Two-Way Paging Applications," *IEEE J. Solid-State Circuits, vol. 33, no.12, Dec. 1998*

[3] H.Darabi and A.A.Abidi, "Noise in RF-CMOS Mixers: A Simple Physical Model," *IEEE J. Solid-State Circuits, vol. 35, no.1, Jan. 2000*

[4] H.Meyr and G. Ascheid, *Synchronization in Digital Communications*, New York: Wiley, 1990.

[5] M. Tiebout, "Design and Optimization of RFCMOS-Circuits for Integrated PLL's and Synthesizers," in the 9th Workshop on *Advances in Analog Circuit Design*, Apr. 2000.